REMARKS

Examiner Dang is thanked for his thorough examination of the Subject Patent Application. Independent Claims 1 and 16 have been made to more clearly describe this invention and in so doing clearly show distinction from Examiners cited prior art. Amended Claims 1 and 16 now describe a conductive layer, an overlying amorphous silicon layer, and a metal layer all being **formed of a single material.** These amended Claims now clearly precludes the use of any material, such as an oxide or another conductive layer such as TiN or TaN, formed between the conductive and amorphous silicon layers.

Regarding the rejection of 1 - 6, 9 - 12, and 14, under 35 USC 103(a) as being unpatentable

over Bai et al, in view of Despande et al, it should be noted that applicants now amended Claim 1, clearly states that an amorphous silicon layer, formed of a single material, is deposited **directly** on the underlying conductive layer, also formed of a single material, **wherein this same underlying conductive layer directly overlays the gate insulator layer without the use of any interceding materials located between the amorphous silicon layer and underlying conductive layer .** In the Bai prior art, as Examiner agrees, layer 208 and layer 204 sandwich barrier layer 206. In direct contrast applicant's counterpart layers, layers 4a and 3a as shown in applicants Fig 1 are formed directly on each other without a sandwiched barrier layer such as shown in the Bai invention. This is now clearly described in amended Claims 1 and 16. This major process difference results in a Bai process wherein a silicon shape is formed on an oxide or barrier layer 206, which in turn overlays a conductive shape, with the oxide or barrier shape

remaining as a component of the Bai invention whereas applicant's final metal silicide shape is formed directly on an underlying conductive layer. The Bai art probably needed the oxide layer as a barrier to prevent consumption of the conductive layer during salicide formation wherein applicant's unique process featured consumption of an amorphous silicon shape directly on an underlying conductive shape without the use of an insulator or barrier layer, without risk to, or consumption of underlying conductive material. The Despande et al prior art only describes some process details similar to applicants's however no combination of the Bai and Despande prior art can result in applicant's unique process sequence in which an amorphous silicon shape, formed **directly** on the underlying conductive shape which in turn directly interfaces the underlying gate insulator. The major process feature, not including a layer between an overlying amorphous silicon layer and an underlying conductive layer on a gate insulator layer, **without the use of a intervening barrier or oxide layer**, results in a less complex and cheaper process than the process described in the Bai invention. Applicant's process described in amended independent Claims 1 and 16, featuring a metal silicide shape formed **directly** on the underlying conductive shape which in turn directly overlays a gate insulator layer, is novel and different the Bai process which describes the use of an intervening barrier or oxide layer between the metal silicide shape and the conductive shape which in turn interfaces the gate insulator layer. Therefore reconsideration of independent Claim 1 as well as all referencing dependent Claims, (2 - 12, and 14 - 15), is requested.

The same argument, formation of an amorphous silicon layer or shape, formed **of a single**

material, directly on an underlying conductive layer, which is also formed of a single material, which in turn directly interfaces a gate insulator layer, **thus precluding the use of underlying insulator barrier layer** as shown in the Bai prior art, is used to argue the rejection of Claims 16 - 21, and 24 - 28, under 35 USC 103 (a) as being unpatentable Bai taken with Despande, in further view of Wieczorek. Again no combination of the above prior art describe the critical feature of forming amorphous material, formed of a single material, directly on the conductive material which is also formed of a single material and which in turn directly interfaces the gate insulator layer, without intervening barrier material. Again the arguments presented for independent Claim 1, is employed wherein the Bai prior art shows the silicon layer which is used for metal silicide formation, interfacing a barrier layer 206, unlike applicants process in which the silicon layer used for metal silicide formation overlays the conductive layer which directly overlays the gate insulator layer .Therefore reconsideration of the rejection of independent Claim 16, and dependent Claims 17 - 21, and 24 - 28, as well as dependent Claims 22 and 31, now referencing a unique independent Claim 16, is requested.

Regarding the rejection of Claims 1 - 4, 6, 7 and 9, under 35 USC 103(a), as being unpatentable over Chau et al (US 5,625,217 B1), in view of Nguyen et al (US 6,084,279), is again addressed via highlighted amended independent Claim 1. No combination of the above prior art describe **an amorphous silicon shape, (formed of a single material) and formed directly on the underlying conductive shape ,(also formed of a single material) which in turn directly overlays a gate insulator layer, wherein an amorphous silicon layer used to**

form the amorphous silicon shape is totally consumed during salicide formation. It is obvious the Chau prior art does not totally consume the amorphous silicon layer overlying a conductive layer, therefore only forming metal silicide on an unconsumed portion of the amorphous silicon layer. Therefore the Chau prior art will not result in the low gate resistance and no polysilicon depletion obtained via applicants process in which all high resistance material is consumed during the silicidation procedure Therefore it is strongly believed that the Chau prior art in combination with the above referencing prior art do not lead to a process sequence in which an amorphous silicon shape, formed directly on an underlying conductive shape, (precluding the use of a insulator barrier layer), is totally consumed during the formation of an metal silicide region directly on an underlying conductive shape. Therefore reconsideration of Claims 1 - 4, 6, 7, and 9, as well as dependent Claims 5, 11, 12, 14 and 15, referencing amended independent Claim 1, is requested.

Regarding the rejection of Claims 16 - 22, 24 - 26, and 28, under 35 USC 103(a), as being unpatentable over Chau et al (US 5,625,217 B1), taken with Nguyen et al (US 6,084,279), and Deshpande et al (US 6,512,266 B1) , and further in view of Wieczorek (US 6,274,511 B1), independent Claim 16, has been amended to now describe an amorphous silicon layer, formed of a single material, and an underlying metal layer formed of a single material, employed to form a silicide shape directly on an underlying gate insulator layer wherein the silicide shape is formed via total consumption of amorphous silicon layer, with no intervening material such as a barrier layer formed between the amorphous silicon and metal layers prior to annealing. Therefore it is believed that no combination of the prior art can describe applicant's invention and therefore

reconsideration of Claims 16 - 22, 24 - 26 and 28, as well as dependent Claims 27 and 31, referencing amended independent Claim 16, is requested.

Therefore it is respectfully suggested that the combinations of these various references cannot be combined without reference to applicant's own invention. None of the applied references address the problem of forming a silicide layer directly on an underlying gate insulator layer wherein the components of the silicide layer an amorphous silicon layer and an underlying conductive layer were formed of a single material. Applicant has claimed his process in detail. The processes of Figs. 1- 8 and Claims 1 - 12, 14 - 28 and 31, are both believed to be novel and patentable over these various references because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination, We therefore request Examiner Dang to reconsider his rejection in view of these arguments and the amendments to the Claims.

Dependent Claims 13, and 29 - 30, have previously been cancelled.

Allowance of all Claims (1- 12, 14 - 28, 31) is requested.

It is requested that should Examiner Dang not find that the Claims are now Allowable that he call the undersigned attorney at 845-452-5863, to overcome any problems preventing allowance.

Respectfully submitted,

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